REMARKS

Claims 1-7 were previously pending in this application. Claims 1-5 were indicated to be allowable. Claims 6 and 7 are rejected.

The Office Action rejected claims 6 and 7 under 35 U.S.C. §103(a) as being unpatentable over Aleksic (5,995,736). Applicant respectfully traverses this rejection.

With regard to claim 6, the Office Action states that Aleksic does not expressly disclose a subsequent phase for simulating the loaded modeling files as claimed. The Office Action asserts that it would have been obvious at the time of the invention to modify Aleksic to use connection files "for generation of hardware design simulation codes for subsequent phase of simulation of loaded modeling files because such simulation information is extracted and connected to become available for subsequent simulation at the circuit level for those skilled in the art to utilize such available resources."

With regard to claim 7, the Office Action takes an inconsistent position. Page 4 of the Office Action states that Aleksic does not expressly disclose simulating the loaded modeling files for a subsequent simulation phase, as claimed. The Office Action asserts that it would have been obvious to modify Aleksic to use connection files "for generation of hardware design simulation codes for subsequent phase of simulation of loaded modeling files." However, the Office Action later asserts, at the last paragraph on page 6, that Aleksic actually discloses using the function model and its states "for subsequent simulation at the circuit level." This statement is inconsistent with the initial position on page 4 that Aleksic fails to disclose simulating the loaded modeling files for a subsequent simulation phase. Indeed, the Office Action has acknowledged that Aleksic fails to disclose this limitation by changing the rejection of claim 7 under 35 U.S.C. §102 to a rejection under 35 U.S.C. §103.

Further, there is no legally sufficient motivation to modify Aleksic as set forth in the Office Action. Aleksic contains no teaching or suggestion to use the output of the behavioral model as an input to the hardware model. Indeed, Aleksic actually teaches away from modifying the reference in this manner. Aleksic explicitly discloses generating and testing the behavioral model and hardware model in parallel. The Office Action has pointed to nothing in Aleksic or any other reference that would suggest modifying the explicit teaching of Aleksic in order to test the hardware model subsequent to the testing of the behavioral model. Thus, one of ordinary

skill in the art would not have been motivated to modify Aleksic in the manner suggested in the Office Action.

Assuming, *arguendo*, that one were to modify Aleksic in the manner suggested in the Office Action, the reference would still fail to teach or suggest all the limitations of claim 6 and claim 7.

Claim 6 is directed to a computer system for simulating an ASP. The computer system comprises first processor means including execution means for simulating a functional model in a high level language and output means for outputting the state of the functional model at the end of a predetermined simulation phase. The computer system further includes means for converting the function, including its state at the end of the predetermined simulation phase, into a simulation language for simulating the ASP at the circuit level.

Aleksic fails to disclose or suggest outputting the state of the function model, converting the function model and its state into a simulation language, and executing the simulation language to simulate the ASP at the circuit level, as recited in claim 6. Nowhere does Aleksic disclose or suggest using the output of the behavioral model as input to the hardware model. Thus, claim 6 patentably distinguishes over Aleksic. Accordingly, it is respectfully requested that the rejection of claim 6 under 35 U.S.C. §103 be withdrawn.

Claim 7 is directed to a modelling file stored on a computer readable medium. The modelling file comprises a first code portion and a second code portion. The first code portion holds a test functions file defining the communication attributes of a processor with a peripheral of an ASP to be simulated and including the state of the test function file after a predetermined simulation phase. The second code portion holds and interface functions file which defines the communication attributes of the peripheral with the processor and the functional attributes of the peripheral and including the state of the interface functions file after the predetermined simulation phase. The code portions are within a circuit level simulation language and are executable by a computer in which the modelling file is loaded to simulate the ASP at circuit level for a subsequent simulation phase.

Aleksic fails to disclose or suggest "that the code portion are within a circuit level simulation language and are executable by a computer in which the modelling files is loaded to simulate the ASP at circuit level for a subsequent simulation phase," as recited in claim 7. Thus,

claim 7 patentably distinguishes over Aleksic. Accordingly, it is respectfully requested that the rejection of claim 7 under 35 U.S.C. §103 be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the applicaton is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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